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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P6623 Total Pages 2

First Named Inventor or Application Identifier Qing Ma

Express Mail Label No. EL034433028US

ADDRESS TO: **Assistant Commissioner for Patents**
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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2. X Specification (Total Pages 20)
   (preferred arrangement set forth below)
   - Cover Sheet
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 25)
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      i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ___ Incorporation By Reference (useable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ___ Microfiche Computer Program (Appendix)
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ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
10. _____ English Translation Document (if applicable)
11. X a. Information Disclosure Statement (IDS)/PTO-1449
    X b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
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ISOLATION STRUCTURE CONFIGURATIONS FOR MODIFYING STRESSES IN SEMICONDUCTOR DEVICES
Inventors: Ma et al.
Our Reference: 42390.P6623

Respectfully submitted,

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Serial/Patent No.: Not Yet Assigned Filing/Issue Date: August 13, 1999
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Date Mailed: August 13, 1999 Docket Due Date: ***

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PATENT
Ref. No. P6623

Express Mail No. EL034433028US

APPLICATION FOR UNITED STATES PATENT

FOR

ISOLATION STRUCTURE CONFIGURATIONS FOR MODIFYING STRESSES IN SEMICONDUCTOR DEVICES

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ISOLATION STRUCTURE CONFIGURATIONS FOR MODIFYING STRESSES IN SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to apparatus and methods for modifying stresses in semiconductor devices. In particular, the present invention relates to modifying isolation structure configurations, such as trench depth and isolation materials used, to either induce or reduce tensile and/or compressive stresses on an active area of MOS semiconductor devices.

State of the Art: Semiconductor integrated circuits are formed by chemically and physically forming circuit components in and on a semiconductor substrate. These circuit components are generally conductive (e.g., for conductor and resistor fabrication) and may be of different conductivity types (e.g., for transistor and diode fabrication). Thus, when forming such circuit components, it is essential that they are electrically isolated from one another, wherein electrical communication between the isolated circuit components is achieved through discrete electrical traces.

Various techniques have been developed for electrically isolating integrated circuit components formed in the semiconductor substrate. One such technique is known as trench isolation. The trench isolation technique involves forming a channel or trench in the semiconductor substrate, usually by etching techniques well known in the art. The trench is formed to surround the circuit components to be isolated and filled with a dielectric material, thereby electrically isolating the circuit components.

FIGs. 22 and 23 illustrate in side cross-sectional view and in top plan view, respectively, components of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor). As shown in FIG. 22, a source region 202 and a drain region 204 are implanted in a semiconductor substrate 206. The source region 202 and the drain region 204 may be implanted with either a p-type material, such as boron, to form a pMOS (p-channel Metal Oxide Semiconductor) transistor or an n-type material, usually phosphorous and/or arsenic, to form an nMOS (n-channel Metal Oxide Semiconductor) transistor.

A gate structure 208 spans a region of the semiconductor substrate 206 between the source region 202 and the drain region 204. An exemplary gate structure 208 comprises

a conductive material 212 electrically isolated with dielectric spacers 214 and 214'adjacent the source region 202 and the drain region 204, a lower dielectric layer 216, and a cap layer 218.

The source region 202 and the drain region 204 are isolated with an isolation structure 222 (i.e., a dielectric-filled trench) extending into the semiconductor substrate 206, preferably beyond the depth of the source region 202 and the drain region 204, as shown in FIG. 22. The isolation structure 222 surrounds the source region 202 and the drain region 204, as shown in FIG. 23, to form an island or active area 224. The material which form the gate structure 208 extends beyond the active area 224 to other semiconductor device components (not shown).

It has been reported in literature that stresses on an active area can significantly effect the performance of MOS devices. Hamada in "A New Aspect of Mechanical Stress Effects in Scaled MOS Device", IEEE Transactions on Electron Devices, vol. 38 (1991), pp. 895-900 illustrated that stresses of the order of 100 MPa can affect performance by a few percent. In the reported experiments, well-controlled uniaxial stresses were applied on MOS devices by using a 4-point bending technique. The stresses were applied both parallel and perpendicular to the channel current direction and for both nMOS and pMOS devices. The results showed that for nMOS devices, tensile stress in both directions improves performance, while compressive stress degrades performance. These effects have been found to be more significant for long channel nMOS devices. For pMOS devices, tensile stress perpendicular to the channel current direction improves performance, but tensile stress parallel to the channel current direction degrades performance, and vice versa for compressive stress.

Such degradation in performance is particularly a problem for MOS devices in flip-chip packaging configurations. FIG. 24 illustrates a cross-sectional view of such a packaging configuration. With flip-chip packaging configurations, a semiconductor die 232 is electrically attached to a carrier substrate 234, such as a printed circuit board, with the active surface 236 of the semiconductor die 232 facing the carrier substrate 234. The electrical attachment of the semiconductor die active surface 236 to the carrier substrate 234 is generally achieved by refluxing solder balls 238 between the semiconductor die active surface 236 and the carrier substrate 234 to form an electrical connection between

electrical traces on or in the semiconductor die 232 (not shown) and electrical traces on the carrier substrate 234 (not shown). Once electrical attachment of the semiconductor die 232 to the carrier substrate 234 is complete, an underfill material 242 is disposed between the semiconductor die 232 and the carrier substrate 234. The resulting structure is then heated to cure the underfill material 242. However, when the resulting structure is cooled down to room temperature from the underfill cure temperature, a bending curvature develops because the carrier substrate 234 contracts more than the semiconductor die 232 (i.e., due to the thermal expansion mismatch between the carrier substrate 234 and the semiconductor die 232), as shown in FIG. 25. Such bending causes biaxial compressive stresses (illustrated by arrows 248 in FIG. 25) on MOS transistors 246 (shown schematically as rectangles in FIGs. 24 and 25) within the semiconductor die 232.

As previously discussed, these biaxial stresses will degrade nMOS device performance. However, these biaxial stresses will have less of an effect on the performance of a pMOS device due to the cancellation effects of the two perpendicular stress components (i.e., the decrease in performance due to compressive stress perpendicular to the channel current direction is offset by the increase in performance due to the compressive stress parallel to the channel current direction).

Therefore, it would be advantageous to develop a technique to effectively induce or reduce tensile and/or compressive stresses on the active area of a MOS device to improve the operating performance thereof, while utilizing commercially-available, widely-practiced semiconductor device fabrication techniques.

SUMMARY OF THE INVENTION

The present invention relates to apparatus and methods for modifying isolation structure configurations, such as trench depth and isolation materials used, to modify (i.e., to either induce or reduce) tensile and/or compressive stresses on an active area of a semiconductor device. In specific, the present invention relates to a semiconductor device having an active area formed in a semiconductor substrate and an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein the isolation structure substantially

surrounds the active area, and wherein at least a portion of the isolation structure is adapted to modify stresses incurred on the active area.

The modification of isolation structure configurations is an effective technique of controlling stresses on a semiconductor device active because the isolation structure is on the same relative plane as the active area and, of course, any device structures formed therein. This shared plane allows for a direct transfer or abatement of stresses incurred on the active area due to packaging or other external stress sources.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings to which:

FIGs. 1 and 2 are side cross-sectional and top plan views, respectively, of an nMOS device having stress modifying isolation structures for accommodating compressive stress, according to the present invention;

FIG. 3 is a side cross-sectional view of the nMOS device of FIGs. 1 and 2 under compressive stress, according to the present invention;

FIG. 4 is a stress model of the effect of the effect of compressive stress applied to a semiconductor die;

FIGs. 5 and 6 are side cross-sectional and top plan views, respectively, of a pMOS device having stress modifying isolation structures for optimizing pMOS performance when under compressive stress, according to the present invention;

FIG. 7 is a cross-sectional view of a back-bonded packaging configuration;

FIG. 8 is a cross-sectional view of the back-bonded packaging configuration of FIG. 7 under stress due to the thermal expansion mismatch;

FIG. 9 is a top plan view of a pMOS device having stress modifying isolation structures for optimizing pMOS performance when under tensile stress, according to the present invention;

FIG. 10 is a side cross-sectional view of a pMOS device having stress modifying isolation structures when under tensile stress, according to the present invention;

FIGs. 11 and 12 are side cross-sectional and top plan view, respectively, of an nMOS device having tensile stress-inducing, dielectric material disposed in an isolation structure, according to the present invention;

FIG. 13 is a top plan view of a pMOS device having tensile stress-inducing and compressive stress-inducing, dielectric material disposed in an isolation structure, according to the present invention;

FIG. 14 and 15 is a model structure and a graph of the results of a numerical simulation using the finite element method for the model structure, respectively, according to the present invention;

FIG. 16 and 17 are side cross-sectional and top plan views, respectively, of an nMOS device having deep isolation structures for accommodating compressive stress, according to the present invention;

FIG. 18 is a side cross-sectional view of a pMOS device having deep isolation structures, according to the present invention;

FIG. 19 is a top plan view of a pMOS device having stress modifying isolation structures for optimizing pMOS performance when under compressive stress, according to the present invention;

FIG. 20 is a top plan view of a pMOS device having stress modifying isolation structures for optimizing pMOS performance when under tensile stress, according to the present invention;

FIG. 21 is a side cross-sectional view of an isolation structure having a conformal barrier layer, according to the present invention;

FIGs. 22 and 23 are side cross-sectional and top plan views, respectively, of components of a MOSFET, as known in the art;

FIG. 24 is a side cross-sectional view of a flip-chip packaging configuration, as known in the art; and

FIG. 25 is a side cross-sectional view of the flip-chip package configuration of FIG. 24 bending under thermal expansion mismatch stresses, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1–21 illustrate various views of the present invention, these figures are not meant to portray semiconductor devices in precise detail. Rather, these figures illustrate semiconductor devices in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between the figures retain that same numeric designation.

It is recognized that it would be advantageous to modify the stresses acting upon the active area of a MOS device in order to improve performance. Such stress modification might be achieved at the packaging level by applying stresses to the semiconductor die. However, semiconductor dice are usually brittle and break easily under stress. Additionally, it is very difficult to apply a uniform stress across an entire semiconductor die. Thus, an attempt to apply a uniform stress across the semiconductor die would likely result in a non-uniform stress which would, in turn, result in undesirable performance variations in the MOS devices across the semiconductor die.

FIGs. 1 and 2 illustrate an embodiment of the present invention for an nMOS device 100. The nMOS device 100 comprises an n-type source region 102 and an n-type drain region 104, which are implanted into a semiconductor substrate 106, such as a silicon wafer, by any known implantation technique. A gate structure 108 spans a region of the semiconductor substrate 106 between the source region 102 and the drain region 104. Generally, the gate structure 108 comprises a conductive material 112 electrically isolated with dielectric spacers 114 and 114' adjacent the source region 102 and the drain region 104, respectively, a lower dielectric layer 116, and a cap layer 118.

The source region 102 and the drain region 104 are isolated with an isolation structure 122, which extends into the semiconductor substrate 106. The isolation structure 122 surrounds the source region 102 and the drain region 104, as shown in FIG. 2, to form an active area 124. The isolation structure 122 includes a dielectric material 126, which has a lower modulus than the semiconductor substrate 106 (i.e., more compliant than the semiconductor substrate 106). Exemplary low-modulus, dielectric materials 126 include, but are not limited to, polymers and porous oxides. As shown in FIG. 3, when compressive stresses (shown as arrows 128 in FIGs. 2 and 3) are incurred on the semiconductor die, such as through flip-chip packaging stress, the low-modulus,

dielectric material 126 deforms, thereby eliminating or lessening the detrimental effect of the compressive stress 128 on the active area 124. FIG. 4 shows a stress model, which illustrates this effect using the finite element method. FIG. 4 shows that under 100 MPa compressive stress applied to a semiconductor die front surface, the average stress in the active area (the vertical axis) depends on the modulus of the trench dielectric material. The horizontal axis is the active area dimension along the direction of applied stress. Curve A represents a trench filled with a silicon dioxide with a modulus of between about 70 and 80 GPa, as commonly used as a dielectric material in the industry. Curve B represents a similar trench filled with a complaint dielectric material, specifically polyimide with a modulus of about 5 GPa. Thus, FIG. 4 illustrates that compressive stress on the active areas can be reduced by using more compliant dielectric materials. This compressive stress reduction is more significant for smaller dimension active areas.

FIGs. 5 and 6 illustrate another embodiment of the present invention for a pMOS device 130. The pMOS device 130 is similar in structure to the nMOS device 100 illustrated in FIGs. 1 and 2 with the exception that the pMOS device 130 has a p-type source region 132 and a p-type drain region 134, as shown in FIG. 5. As previously discussed for pMOS devices, tensile stress perpendicular to the channel current direction improves performance, but tensile stress parallel to the channel current direction degrades performance, and vice versa for compressive stress. As shown in FIG. 6, to improve the performance of the pMOS device, the low-modulus, dielectric material 126 is placed in the isolation structure 122 parallel to the channel current direction to eliminate or lessen the detrimental compressive stress perpendicular to the channel current direction. Furthermore, a high-modulus (stiff), dielectric material 136 is placed in the isolation structure 122 perpendicular to the channel current direction to translate the beneficial compressive stress parallel (shown as arrows 128) to the channel current direction to the active area 124. The high-modulus, dielectric material 136 should have a modulus equal to or higher than a modulus of the semiconductor substrate 106. Therefore, any stresses incurred on the high-modulus, dielectric material 136 will also be incurred on active area 124 with substantially the same force (shown as arrows 138). Exemplary high-modulus, dielectric materials 136 include, but are not limited to, silicon nitride and silicon dioxide, which are deposited to have compressive stresses.

It is, of course, understood that the use of low-modulus, dielectric material can also improve pMOS device performance in back-bonded packaging configurations. FIGs. 7 and 8 illustrate a back-bonded package 140. With back-bonded packaging configurations, a back surface 142 of a semiconductor die 144 is attached to a carrier substrate 146. Electrical communication between the semiconductor die 144 and the carrier substrate 146 is generally achieved by bond wires 148 extending between electrical traces (not shown) on or in an active surface of the semiconductor die 144 and electrical traces (not shown) on the carrier substrate 146. The attachment of the semiconductor die back surface 142 to the carrier substrate 146 achieved with an adhesive material 152, such as an epoxy resin, as shown in FIG. 7. The resulting structure is then heated to cure the adhesive material 152. However, when the resulting structure is cooled down to room temperature from the adhesive material cure

temperature, a bending curvature develops because the carrier substrate 146 contracts more than the semiconductor die 144 (i.e., due to the thermal expansion mismatch between the carrier substrate 146 and the semiconductor die 144), as shown in FIG. 7. Such bending causes biaxial tensile stresses (illustrated by arrows 154 in FIG. 8) on the MOS transistors (shown schematically as rectangles 156 in FIG. 8) within the semiconductor die 144.

Of course, these biaxial tensile stresses enhance the performance of nMOS devices, but have little effect on the performance of a pMOS device, due to the cancellation effects of the two perpendicular stress components. However, the low-modulus, dielectric material 126 can be used to improve the performance a pMOS device. As shown in FIG. 9, the low-modulus, dielectric material 126 is placed in the isolation structure 122 perpendicular to the channel current direction to eliminate or lessen the detrimental tensile stress parallel to the channel current direction of pMOS device 150. The parallel tensile stress is eliminated or lessened, because when parallel tensile stress (shown as arrows 154 in FIG. 9) is incurred on the semiconductor die, the low-modulus, dielectric material 126 stretches, as shown in FIG. 10, thereby eliminating or lessening the detrimental effect of the tensile stress 128 on the active area 124. Furthermore, referring to FIG. 9, a high-modulus (stiff), dielectric material 136 may be placed in the isolation structure 122 parallel to the channel current direction to translate the beneficial tensile stress perpendicular to the channel current direction to the active area 124 (translated tensile stress shown as arrows 158).

FIGs. 11 and12 illustrate yet another embodiment of the present invention for an nMOS device 160. The nMOS device 160 illustrated in FIGs. 11 and 12 is similar in structure to the nMOS device 100 illustrated in FIGs. 1 and 2. However, with the present embodiment, the isolation structure 122 includes a dielectric material 162, which has tensile stress-inducing properties (e.g., it creates a tensile stress on adjacent structures and/or materials). Exemplary tensile stress-inducing, dielectric materials 162 include, but are not limited to, silicon nitride which has been deposited to have large tensile stresses. As shown in FIG. 11, the tensile stress-inducing, dielectric material 162 creates a tensile stress (shown as arrows 164) on the active area 124 thereby improving the performance of the nMOS device, even when no external stresses are incurred on the

semiconductor die. However, when compressive stresses (shown as arrow 128 in FIG. 12) are incurred on the semiconductor die, the tensile stress-inducing, dielectric material 162 creates the tensile stress (shown as arrows 164) on the active area 124 in a direction opposite the compressive stresses 128, which eliminates or lessens the detrimental effect of the compressive stress 128.

FIG. 13 illustrates a still another embodiment of the present invention for a pMOS device 170. The pMOS device 170 is similar in structure to the pMOS device 130 illustrated in FIGs. 5 and 6. As previously discussed for pMOS devices, tensile stress perpendicular to the channel current direction improves performance, but tensile stress parallel to the channel current direction degrades performance, and vice versa for compressive stress. Thus, to improve the performance of the pMOS device, the tensile stress-inducing, dielectric material 162 is placed in the isolation structure 122 parallel to the channel current direction to eliminate or lessen the detrimental compressive stress perpendicular to the channel current direction. Furthermore, a compressive stress-inducing, dielectric material 166 may be placed in the isolation structure 122 perpendicular to the channel current direction to induce the beneficial compressive stress (shown as arrows 168) parallel to the channel current direction to the active area 124. The compressive stress-inducing, dielectric material 166 creates a compressive stress on adjacent structures and/or materials. Exemplary compressive stress-inducing, dielectric materials 166 include, but are not limited to, silicon nitride and silicon dioxide which are deposited to have compressive stresses. Thus, the configuration shown in FIG. 13 improves the performance of the pMOS device when no external stresses are incurred on the semiconductor die or when biaxial compressive or tensile stresses are incurred on the semiconductor die.

A further embodiment of the present invention involves increasing isolation structure depth to reduce compressive stresses. FIGs. 14 and 15 illustrate a model structure and a graph of the results of a numerical simulation using the finite element method for the model structure, respectively. In FIG. 14, A is the active area width (or length), B is the isolation structure width, H is the trench depth and D is the active area depth. In the simulation, the trench width B was fixed at 0.5 microns (stress incurred on the active area is not significantly sensitive to trench width) and the active region depth

D is fixed at 0.25 um (i.e., a typical active region depth). Thus, the active area width A and isolation structure depth H are variables. FIG. 15 illustrates the simulation results with a dielectric material having a modulus of about 5 GPa, wherein the horizontal axis is the trench depth H, and the vertical axis is the compressive stress in the active area normalized by the semiconductor die/packaging thermal mismatch stress (i.e., applied stress). The simulation was performed for three active area widths (i.e., A=2.0um corresponding to curve A1, A=1.0um corresponding to curve A2, and A=0.5um corresponding to curve A3) covering a range of interest. As FIG. 15 illustrates for all the three active area widths, the compressive stresses decreased and approached zero with an increase of trench depth. Furthermore, it is observed that the smaller the active area width A, the less the active area is affected by the applied stress. The increased trench depth makes the carrier substrate 106 more flexible. Thus, when a dielectric material which is more compliant than the carrier substrate is used, the stress on the active area is decreased. Preferably, the structure should have a trench depth H to active area width A aspect ratio (i.e., H/A) of greater than about 0.5.

FIGs. 16 and 17 illustrates the deep trench embodiment of the present invention for an nMOS device 172. The nMOS device 172 illustrated in FIG. 16 is similar in structure to the nMOS device 100 illustrated in FIGs. 1. However, with the present embodiment, the isolation structure depth is increased to form deep isolation structure 174. The increased depth of the deep isolation structure 174 has been found to reduce compressive stresses on the active area 124. FIG. 17 illustrates a configuration wherein the deep isolation structure 174 surrounds the active area 124. The deep isolation structure 174 includes a dielectric material 178 disposed therein. With the deep isolation structure 174, a standard dielectric material 178, such as silicon dioxide, may be used to isolate the active area 124. However, to further enhance the reduction in compressive stress, the dielectric material 178 may be a low-modulus dielectric material (such as described in regard to FIGs. 1 and 2) or a tensile stress-inducing, dielectric material (such as described in regard to FIGs. 11 and 12).

FIG. 18 illustrates the deep trench embodiment of the present invention for a pMOS device 180 with the deep trenches formed perpendicular to the channel current

direction. The pMOS device 180 illustrated in FIG. 18 is similar in structure to the nMOS device 130 illustrated in FIG. 5.

As illustrated in FIG. 19, when the pMOS device 180 is subjected to biaxial compressive stresses (e.g., flip-chip packaging configurations), the isolation structure depth is increased only in portions 182 of the isolation structure 122 which are parallel to the channel current direction in order to eliminate or lessen the detrimental compressive stresses perpendicular to the channel current direction. In order to further reduce detrimental compressive stresses on the active area 124 perpendicular to the channel current direction, a low-modulus dielectric material (such as described in regard to FIG. 6) or a tensile stress-inducing, dielectric material (such as described in regard to FIG. 13) may be disposed in isolation structure portions 182. Portions 184 of the isolation structure 122 which are perpendicular to the channel current direction are of a depth sufficient to isolate the active area 124, but may translate beneficial compressive stress to the active area 124 parallel to the channel current direction. In order to further translate or induce beneficial compressive stress to the active area 124 parallel to the channel current direction, the isolation structure portions 184, a high-modulus dielectric material (such as described in regard to FIG. 6) or a compressive stress-inducing, dielectric material (such as described in regard to FIG. 13) may be disposed in isolation structure portions 184.

When the pMOS device 190 is subjected to biaxial tensile stresses (e.g., back-bonded packaging configurations), the isolation structure depth is increased for the isolation structure depth is increased only in portions 192 of the isolation structure 122 which are perpendicular to the channel current direction in order to eliminate or lessen the detrimental tensile stresses parallel to the channel current direction, as shown in FIG. 20. In order to further reduce detrimental tensile stresses on the active area 124 perpendicular to the channel current direction, a low-modulus dielectric material (such as described in regard to FIG. 6) or a compressive stress-inducing, dielectric material (such as described in regard to FIG. 13) may be disposed in isolation structure portions 192. Portions 194 of the isolation structure 122 which are parallel to the channel current direction are of a depth sufficient to isolate the active area 124, but may translate beneficial tensile stress to the active area 124 perpendicular to the channel current

direction. In order to further translate or induce beneficial tensile stress to the active area 124 perpendicular to the channel current direction, the isolation structure portions 194, a high-modulus dielectric material (such as described in regard to FIG. 9) or a tensile stress-inducing, dielectric material (such as described in regard to FIG. 13) may be disposed in isolation structure portions 194.

It is also understood, that the introduction of various low-modulus and high-modulus dielectric material, and compressive stress-inducing and tensile stress-inducing, dielectric materials may degrade the interface between the active area and the dielectric material and cause leakage problems. Thus, a thin conformal barrier layer 196, such as a conformal layer of silicon dioxide 196 may be deposited in the isolation structure 122 prior to depositing any of the various dielectric materials 198, as shown FIG. 21.

* * * * *

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

What is claimed is:

1. A semiconductor device, comprising:

an active area formed in a semiconductor substrate; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, and wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area.

2. The semiconductor device of claim 1, wherein said active area further comprises nMOS device components including an n-type source region, an n-type drain region, and a gate structure disposed adjacent said active area between said n-type source region and said n-type drain region.

3. The semiconductor device of claim 2, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench.

4. The semiconductor device of claim 2, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

5. The semiconductor device of claim 2, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

6. The semiconductor device of claim 5, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench.

7. The semiconductor device of claim 5, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

8. The semiconductor device of claim 1, wherein said active area further comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region.

9. The semiconductor device of claim 8, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench parallel to a channel current direction of the pMOS device components.

10. The semiconductor device of claim 9, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

11. The semiconductor device of claim 8, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to a channel current direction of the pMOS device components.

12. The semiconductor device of claim 11, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

13. The semiconductor device of claim 8, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

14. The semiconductor device of claim 8, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

15. The semiconductor device of claim 8, wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

16. The semiconductor device of claim 15, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction.

17. The semiconductor device of claim 15, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction.

18. The semiconductor device of claim 15, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

19. The semiconductor device of claim 15, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

20. The semiconductor device of claim 8, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench perpendicular to a channel current direction of the pMOS device components having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

21. The semiconductor device of claim 20, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

22. The semiconductor device of claim 20, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

23. The semiconductor device of claim 20, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

24. The semiconductor device of claim 20, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

25. A method of forming an stress modifying isolation structure, comprising:

forming a trench in said semiconductor substrate to substantially surround an active area of a semiconductor substrate; and

disposing at least one stress-modifying, dielectric material within at least a portion said trench.

26. The method of claim 25, wherein said disposing said at least one stress-modifying, dielectric material within said at least a portion of said trench comprises disposing a low-modulus, dielectric material within said at least a portion of said trench.

27. The method of claim 25, wherein said disposing said at least one stress-modifying, dielectric material within said at least a portion of said trench comprises disposing a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

28. The method of claim 25, wherein said disposing said at least one stress-modifying, dielectric material within said at least a portion of said trench comprises disposing a high-modulus, dielectric material within said at least a portion of said trench.

29. The method of claim 28, wherein said disposing said at least one stress-modifying, dielectric material within said at least said portion of said trench comprises disposing a compressive stress-inducing, dielectric material within said at least said portion of said trench.

30. A method of forming an stress modifying isolation structure, comprising:

forming a trench in said semiconductor substrate to substantially surround an active area, wherein said active area includes a width and wherein at least a portion of said trench includes a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5; and

disposing at least one dielectric material within at least a portion of said trench.

ABSTRACT

An apparatus and methods for modifying isolation structure configurations for MOS devices to either induce or reduce tensile and/or compressive stresses on an active area of the MOS devices. The isolation structure configurations according to the present invention include the use of low-modulus and high-modulus, dielectric materials, as well as, tensile stress-inducing and compressive stress-inducing, dielectric materials, and further includes altering the depth of the isolation structure and methods for modifying isolation structure configurations, such as trench depth and isolation materials used, to modify (i.e., to either induce or reduce) tensile and/or compressive stresses on an active area of a semiconductor device.

FIG. 1

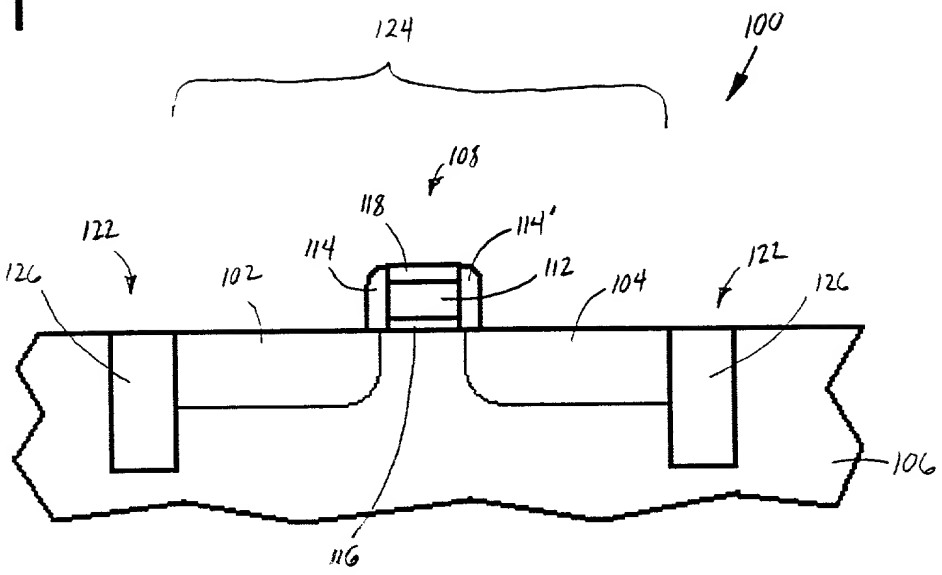

FIG. 2

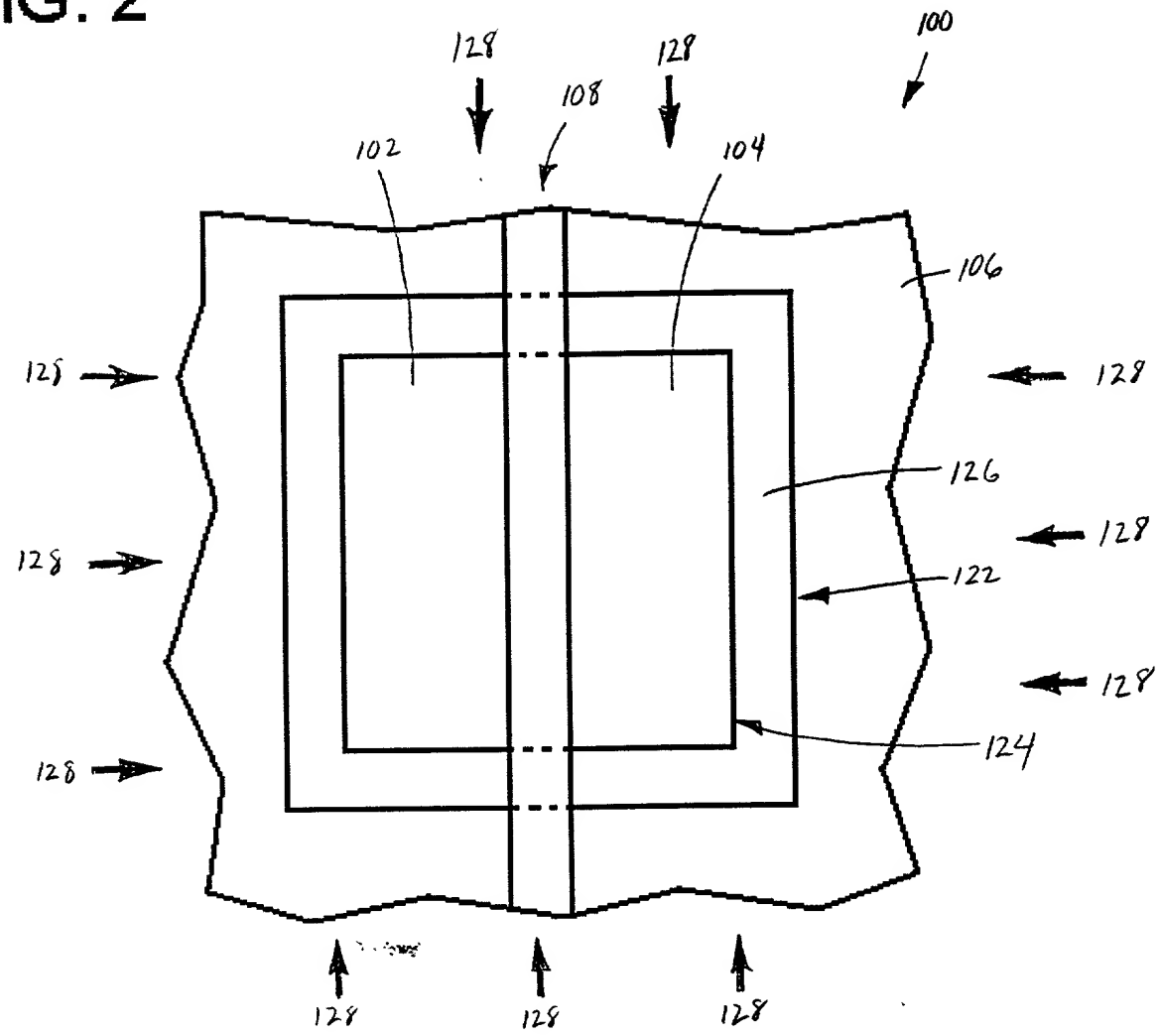
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FIG. 3

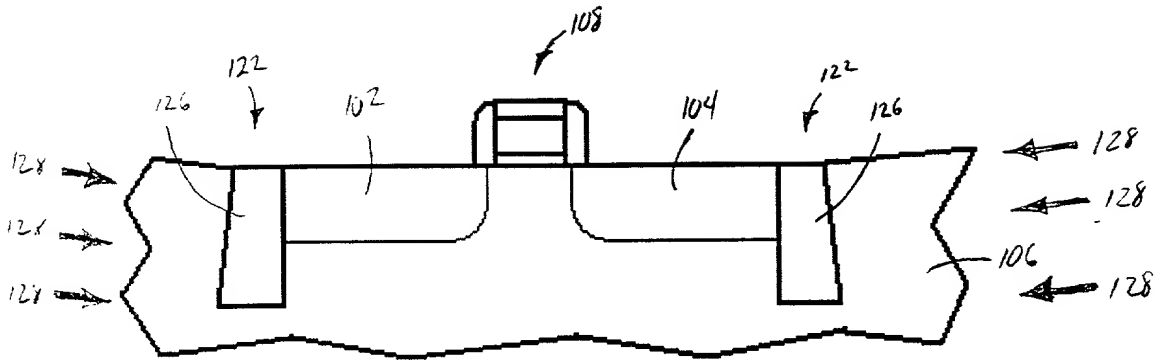
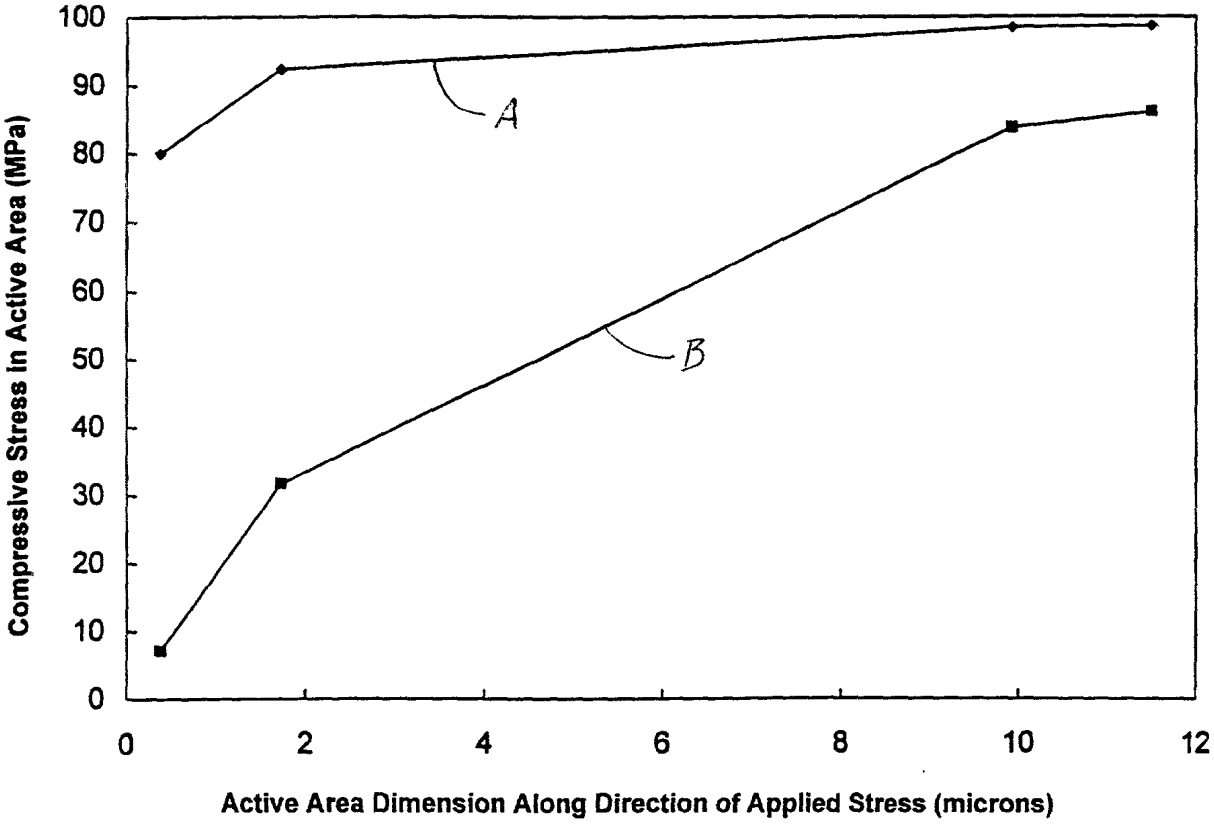


FIG. 4


100
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A
B
Compressive Stress in Active Area (MPa)
Active Area Dimension Along Direction of Applied Stress (microns)

FIG. 5

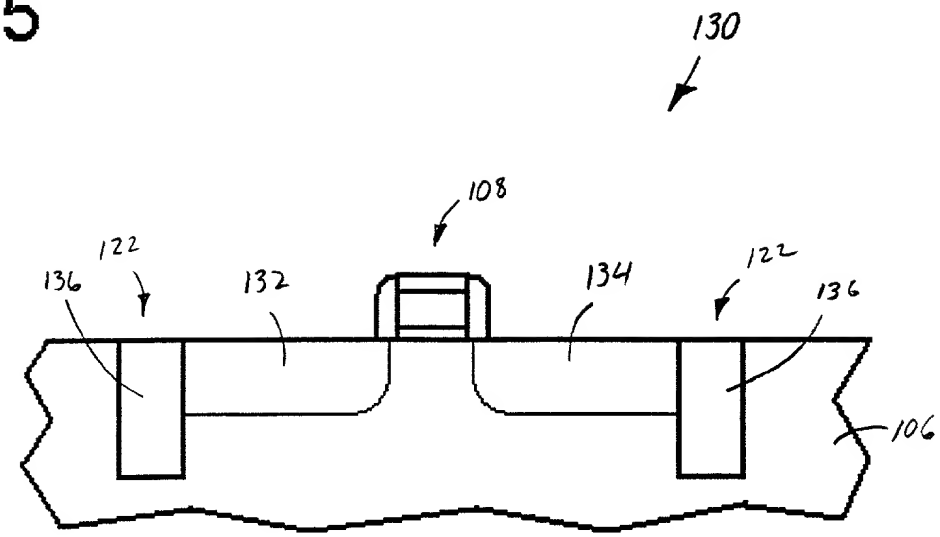

FIG. 6

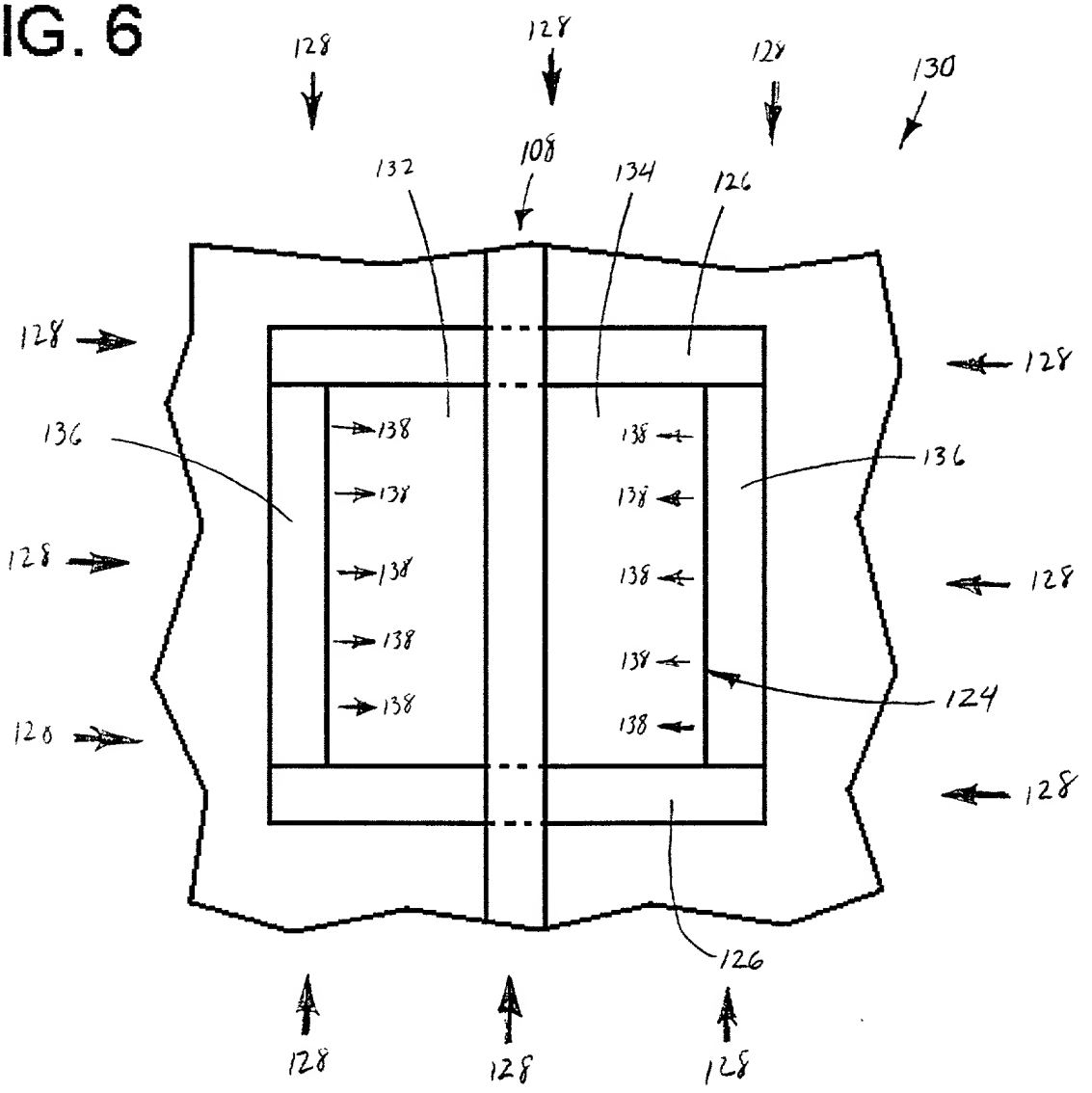
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FIG. 7

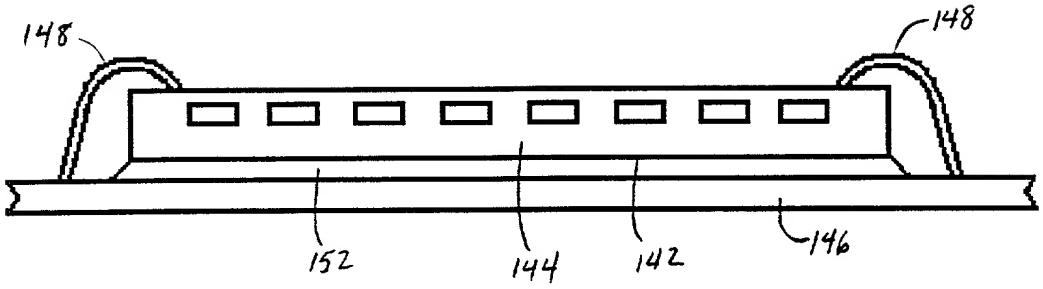

FIG. 8

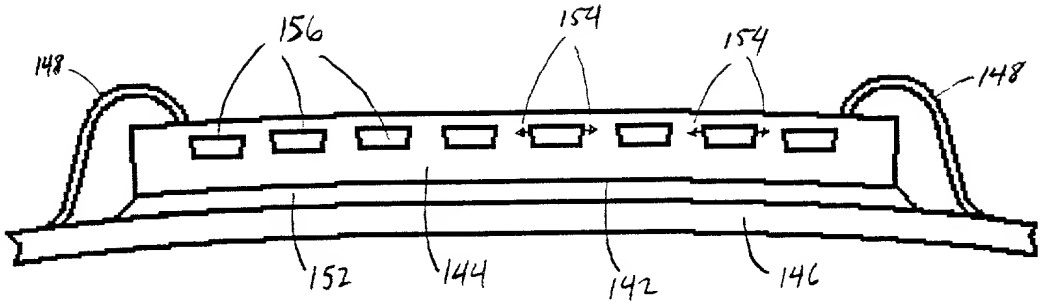

FIG. 9

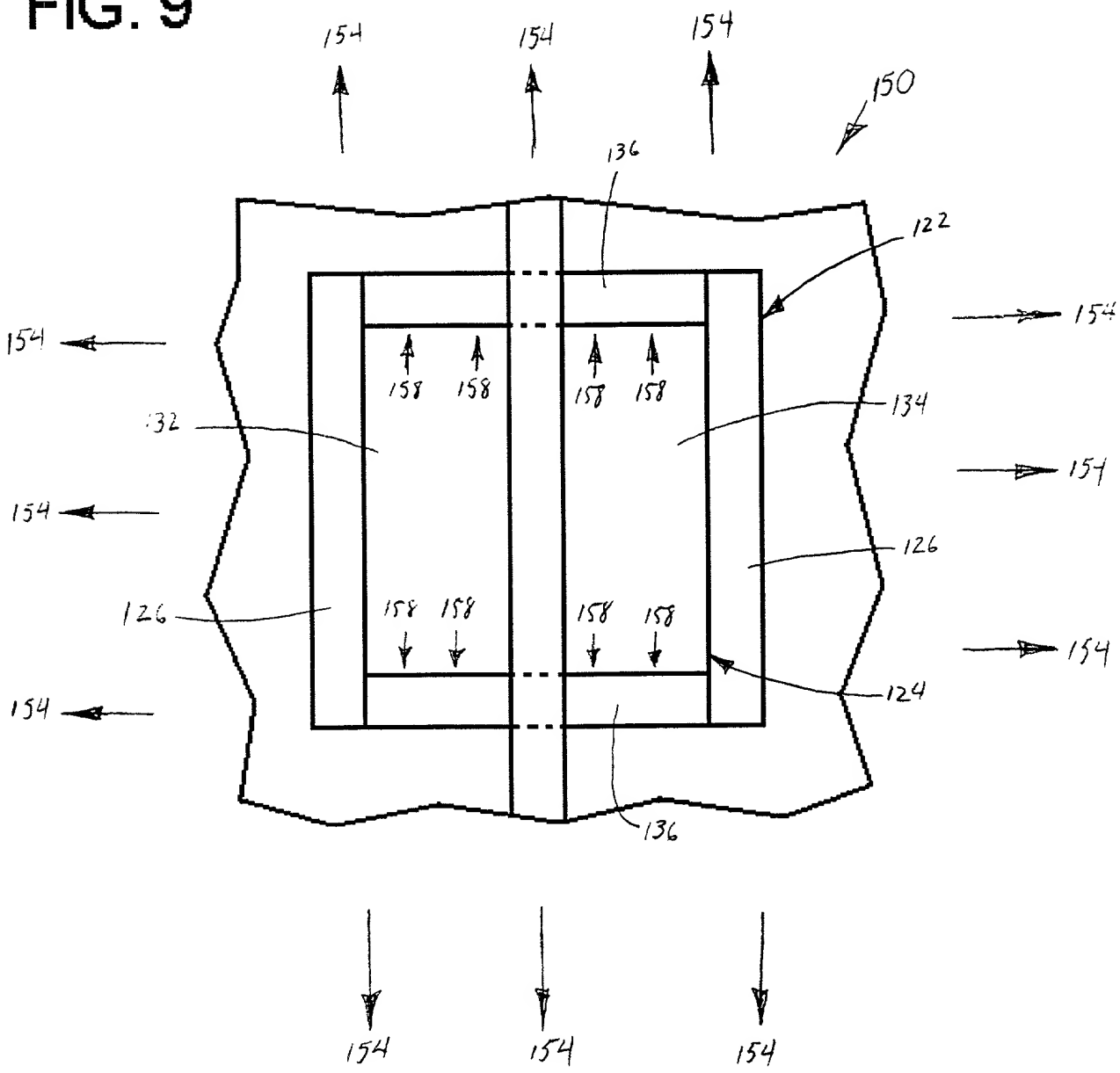
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FIG. 10

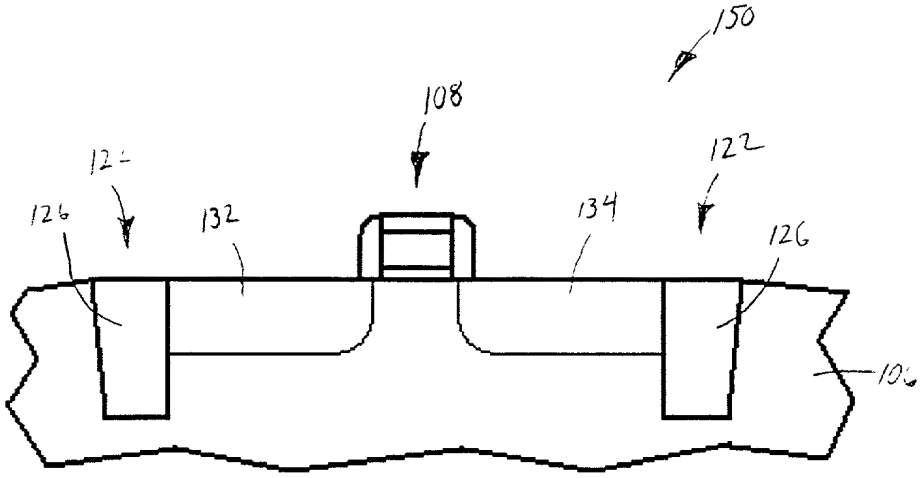

FIG. 11

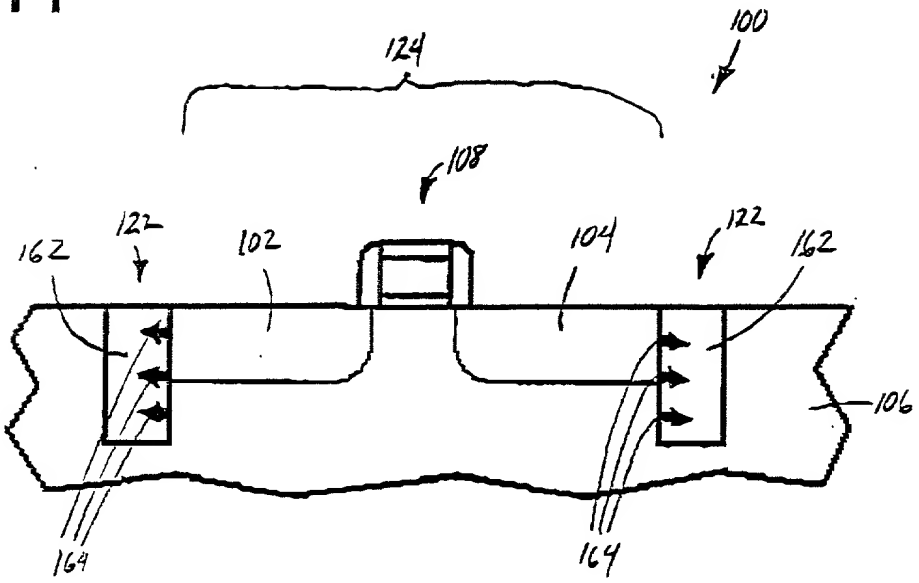

FIG. 12

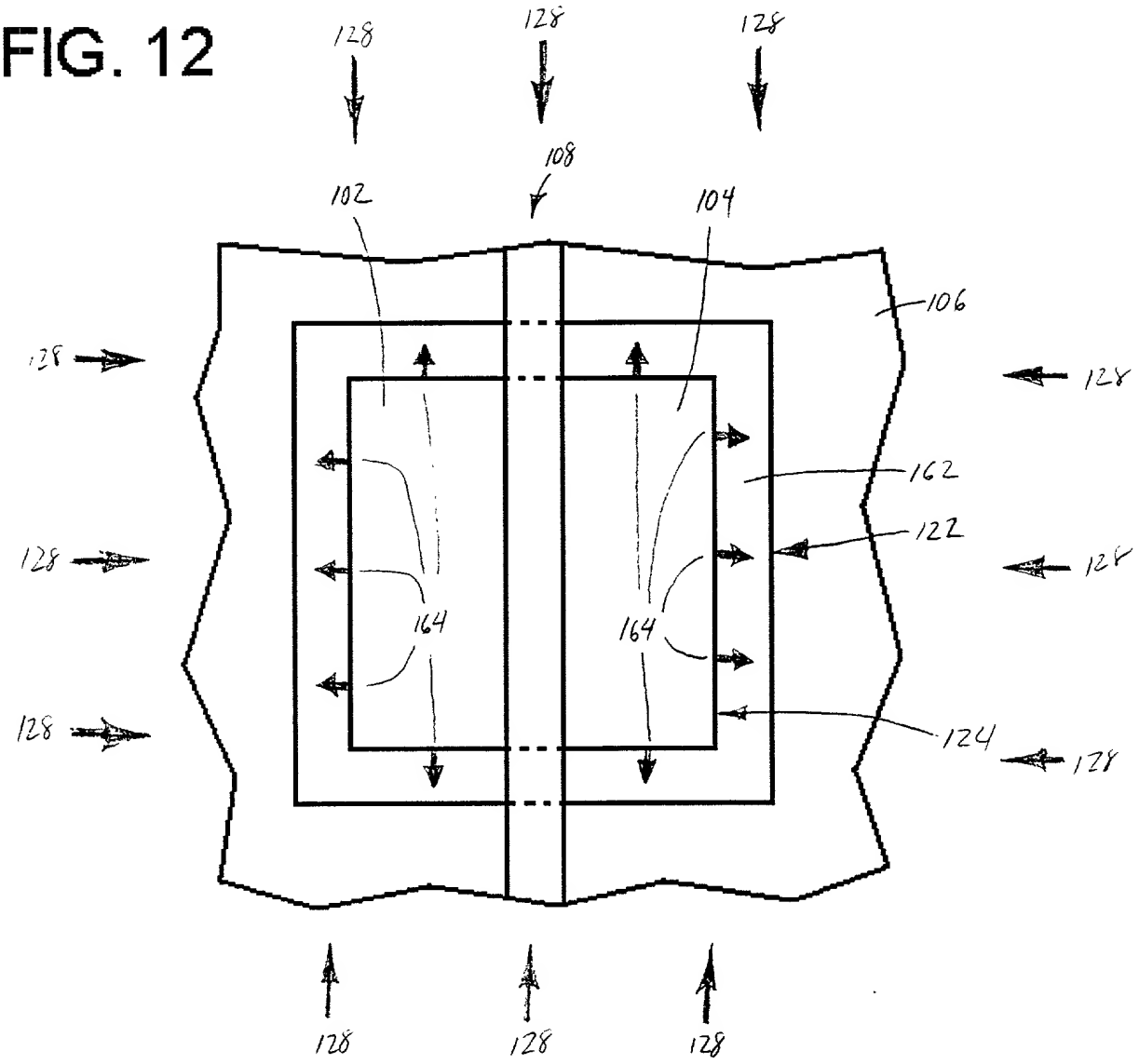
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FIG. 13

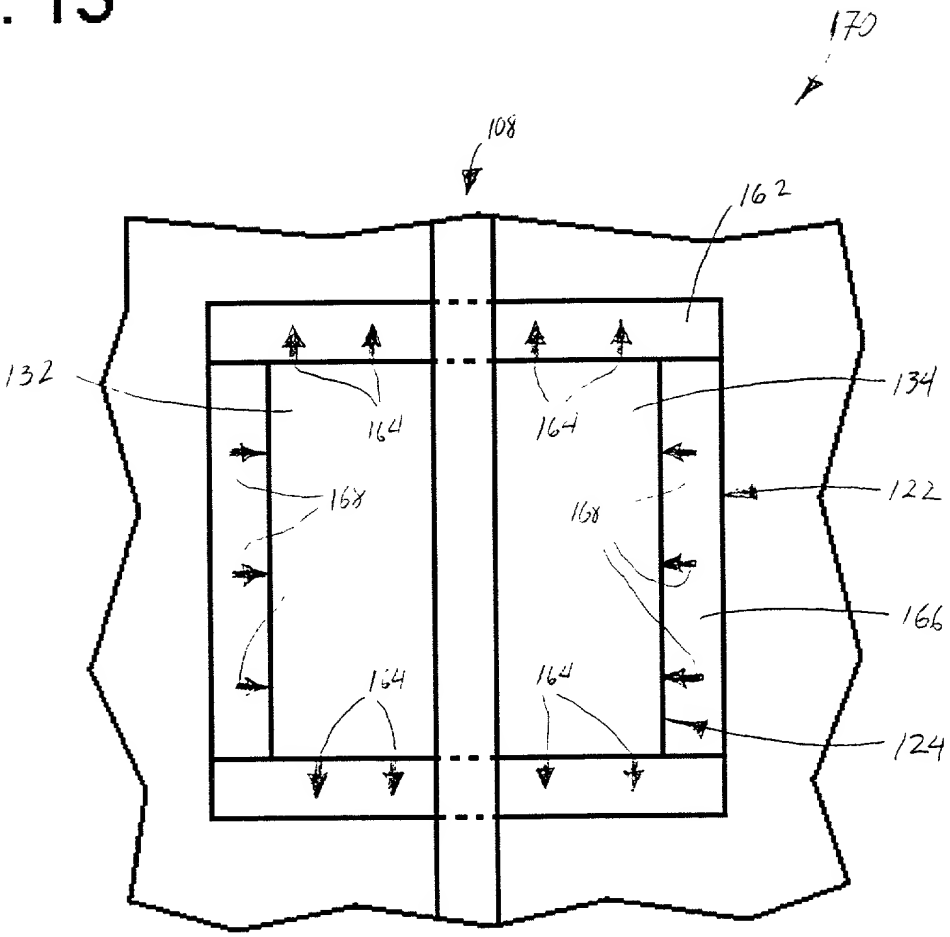


FIG. 14

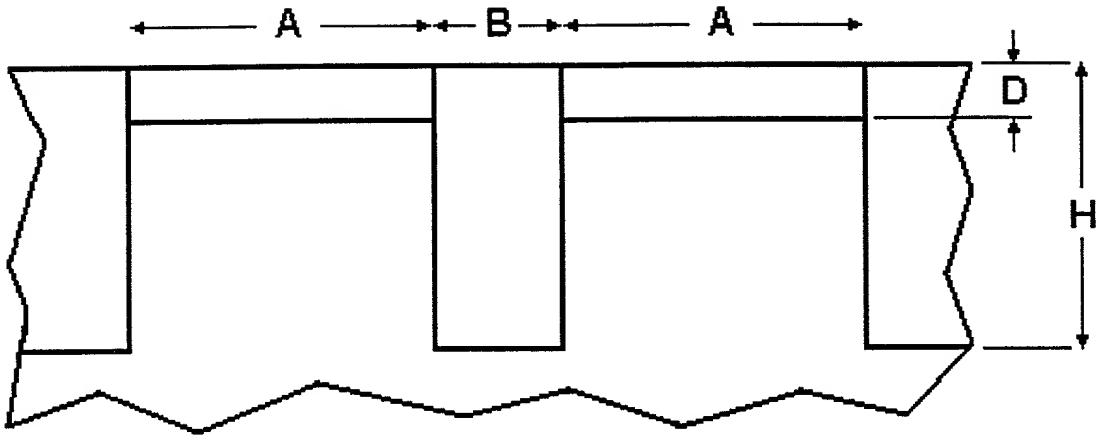


FIG. 15

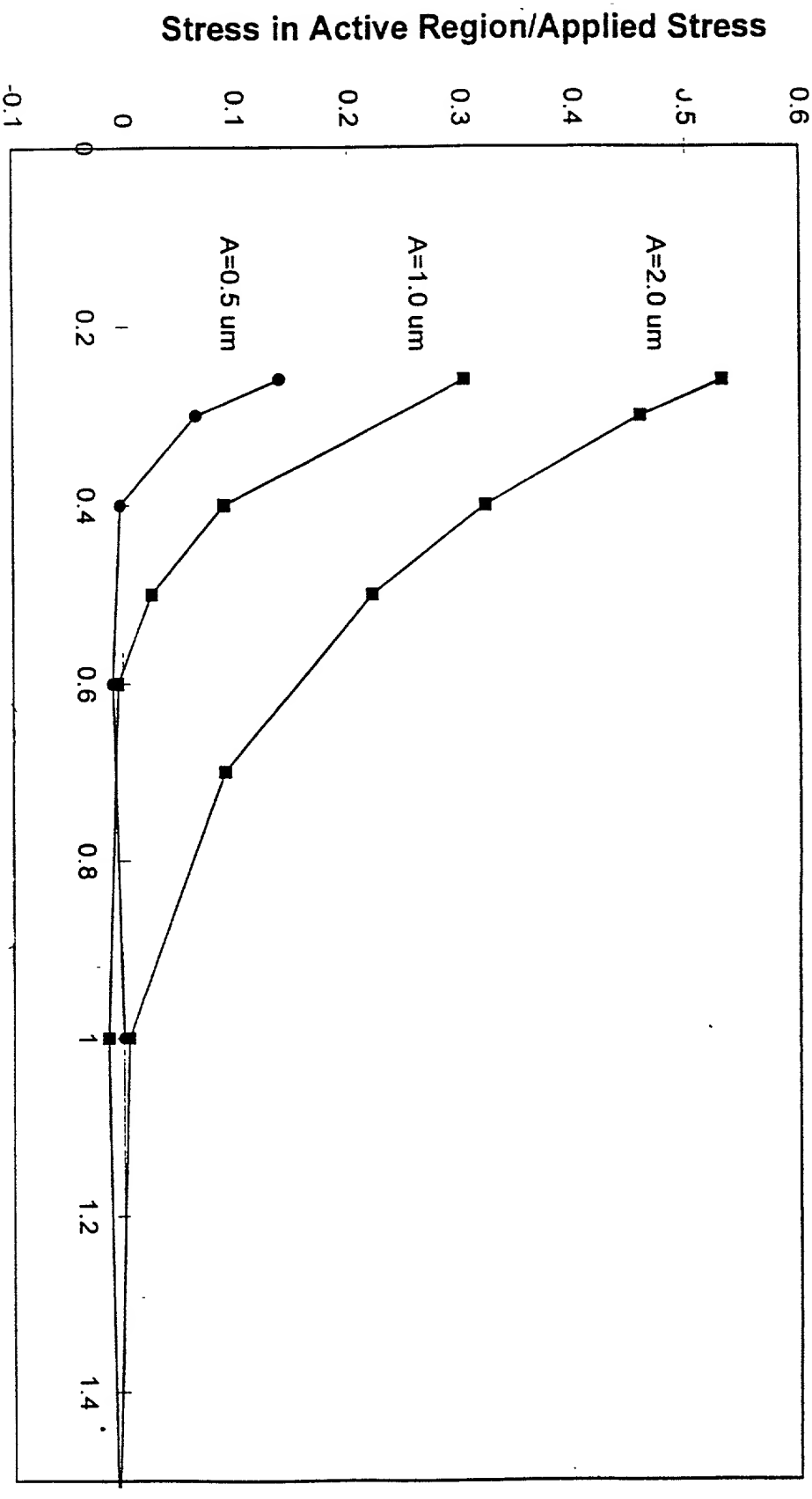

Stress in Active Region/Applied Stress
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
A=2.0 um
A=1.0 um
A=0.5 um
0
0.2
0.4
0.6
0.8
1
1.2
1.4
Trench Depth H (um)

FIG. 16

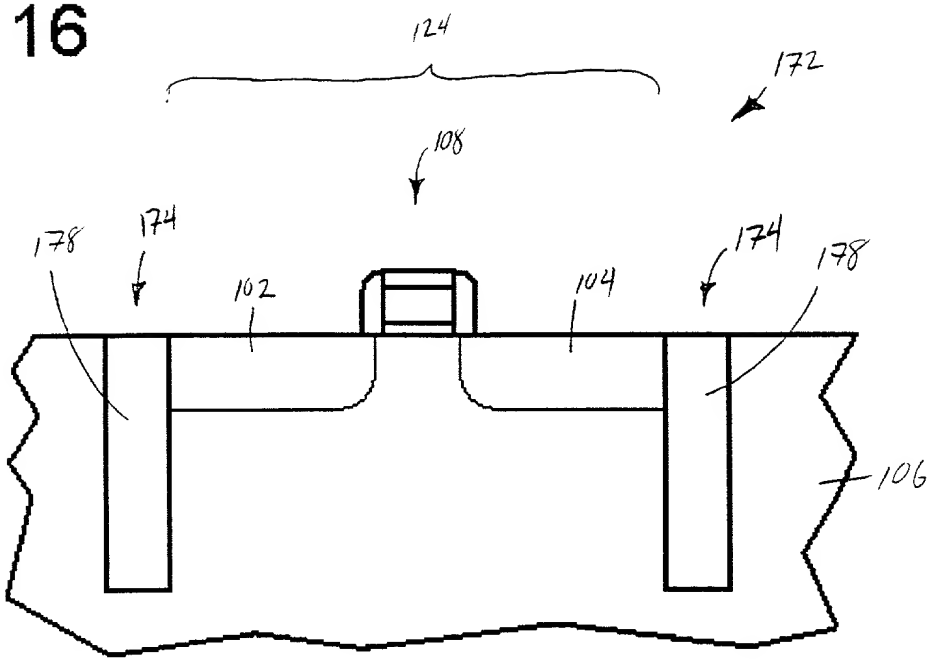


FIG. 17

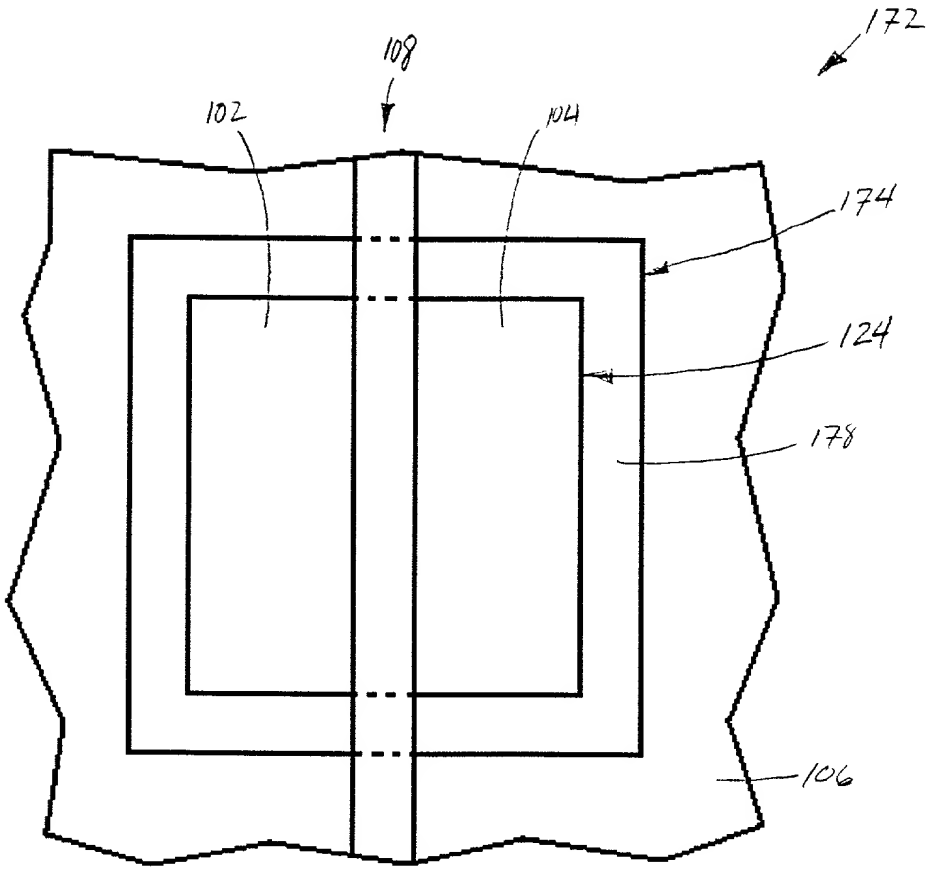


FIG. 18

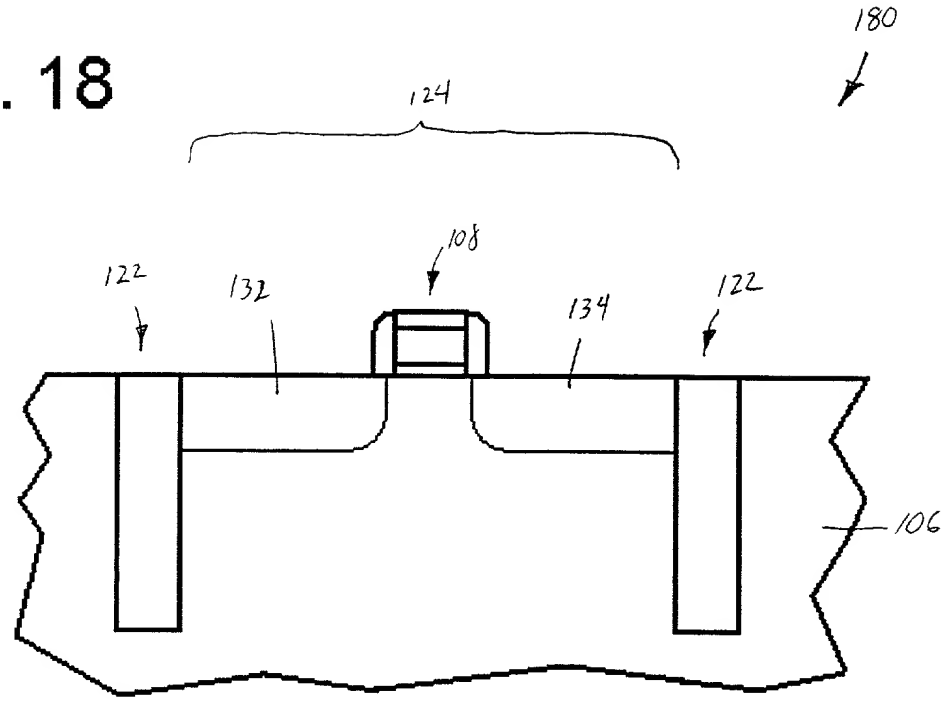


FIG. 19

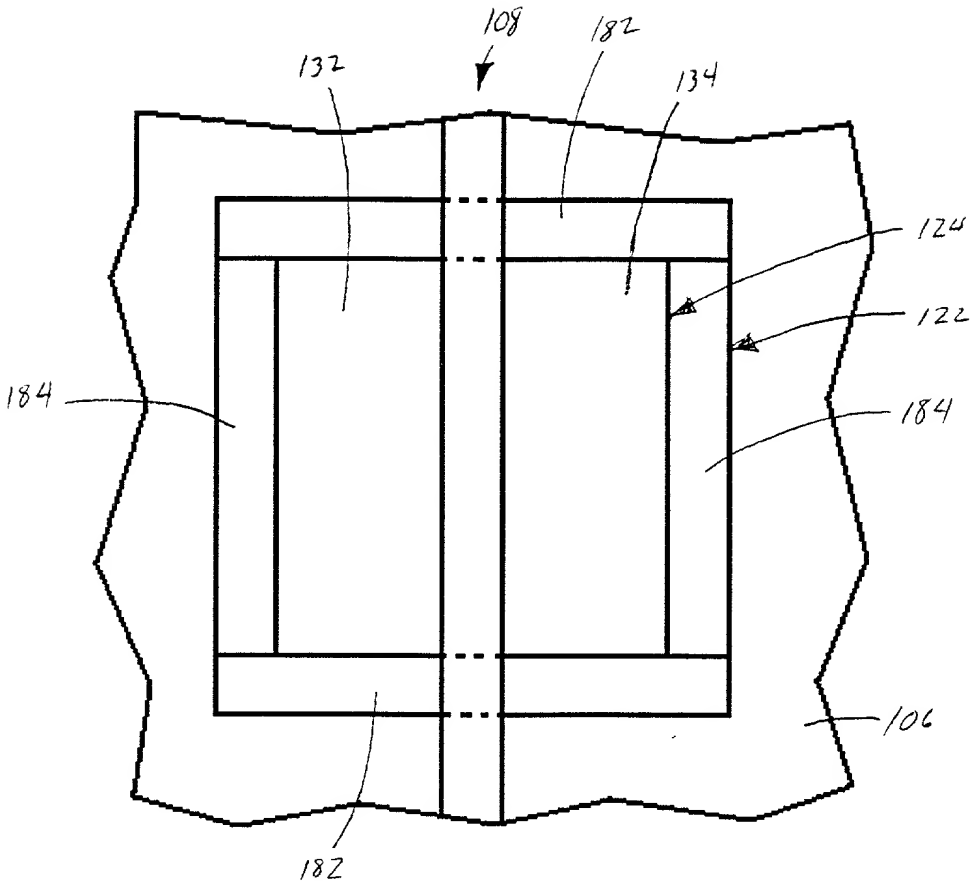


FIG. 20

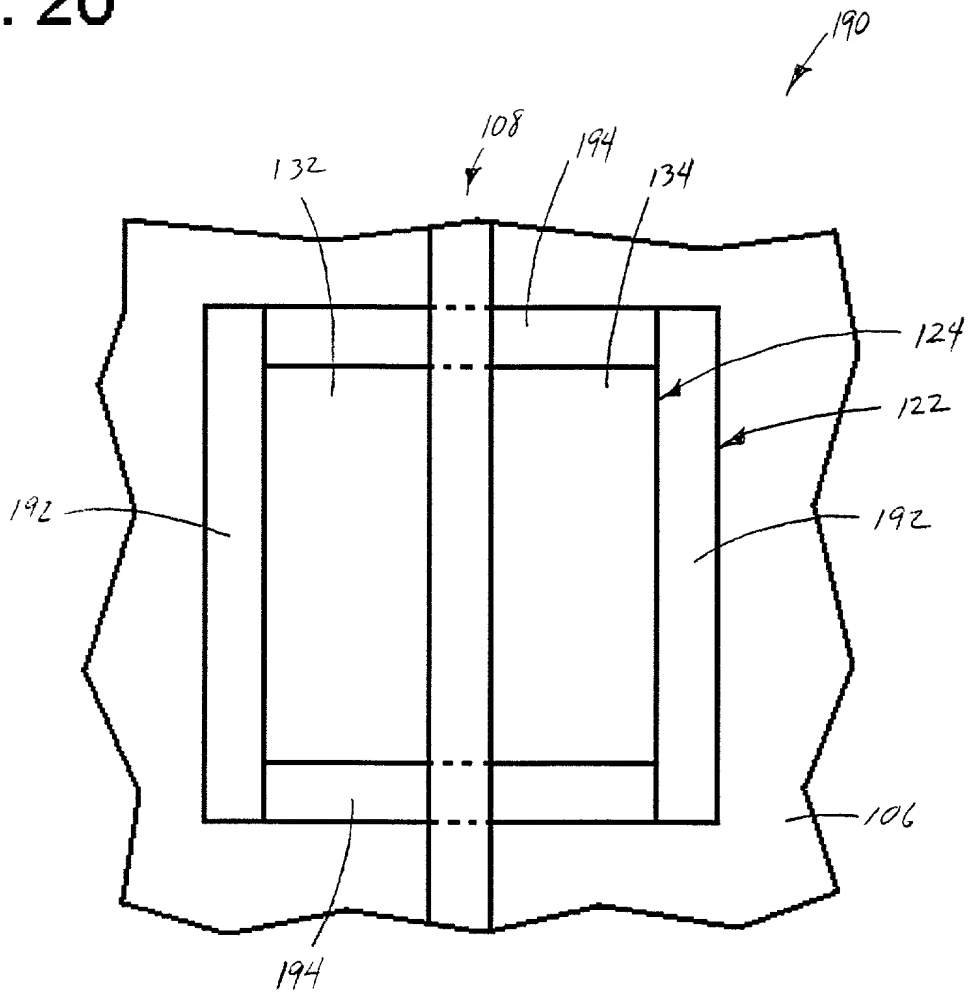


FIG. 21

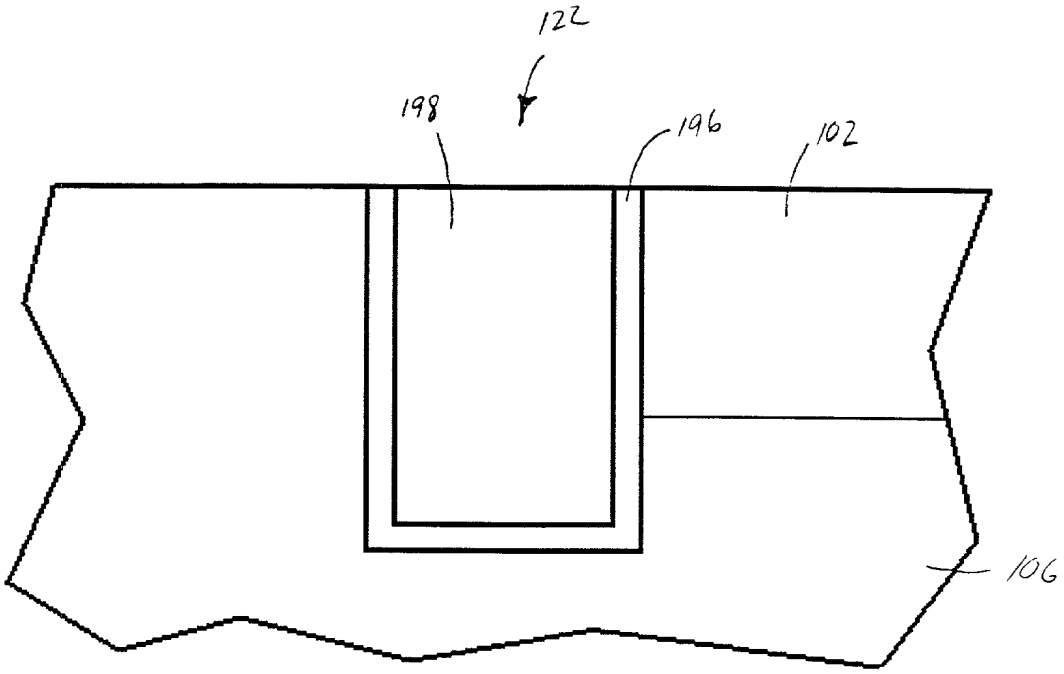


FIG. 22
Prior Art

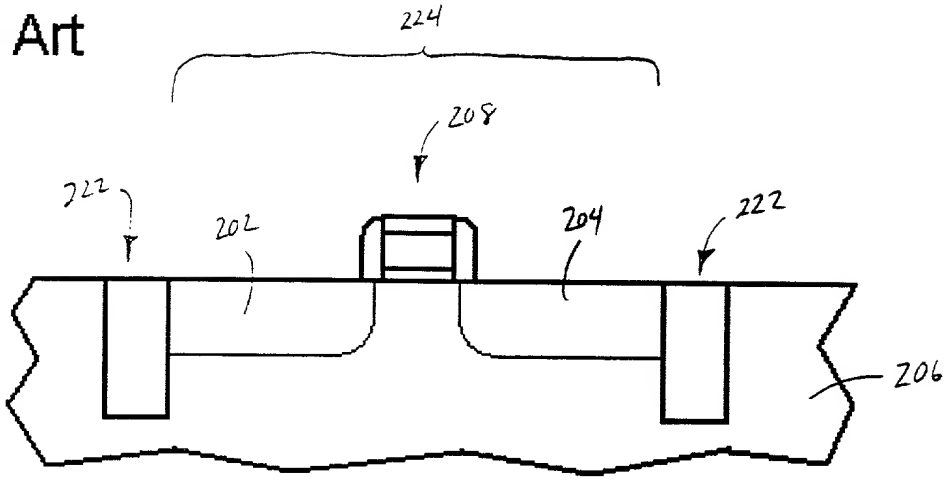


FIG. 23
Prior Art

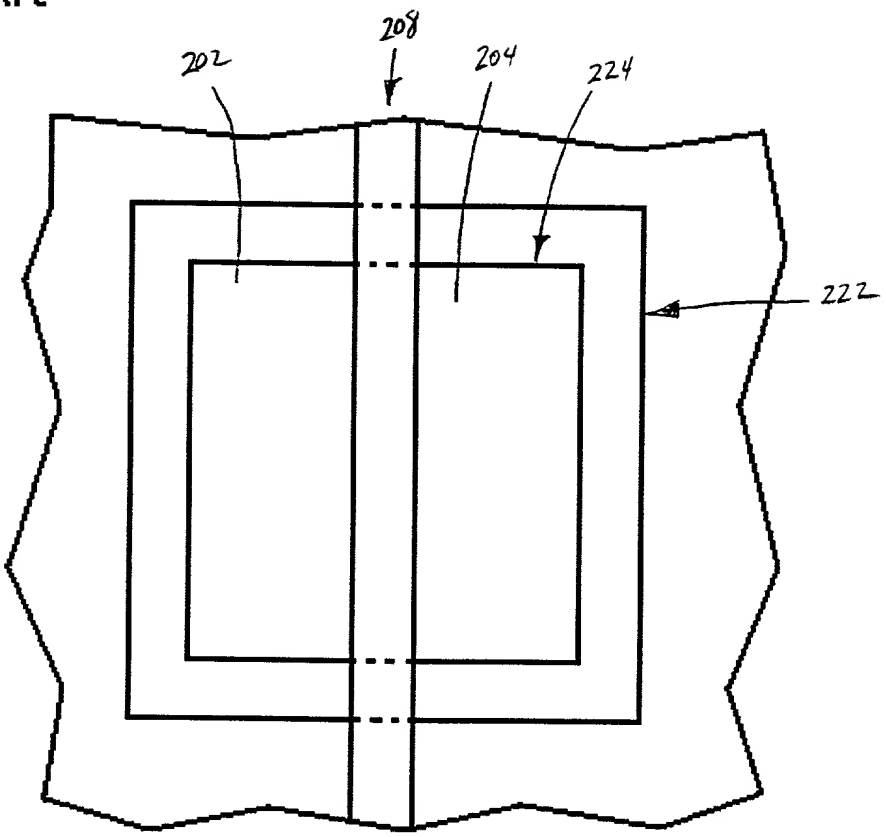


FIG. 24
Prior Art

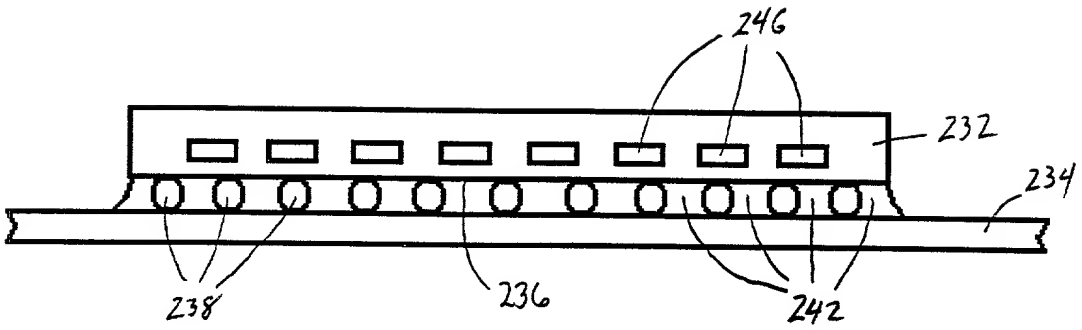
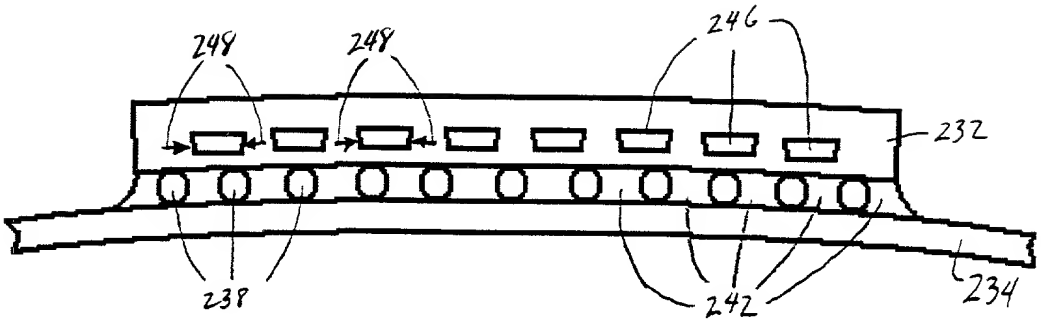


FIG. 25
Prior Art



Attorney's Docket No.: 42390.P6623 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ISOLATION STRUCTURE CONFIGURATIONS FOR MODIFYING STRESSES IN SEMICONDUCTOR DEVICES

the specification of which

XX is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Steven D. Yates, Reg. No. 42,242; Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Jeffrey S. Draeger, Reg. No. 41,000; Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells, Reg. No. P43,256; and Alexander Ulysses Witkowski, Reg. No. P43,280; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Robert G. Winkle, Intel, BLAKELY, SOKOLOFF, TAYLOR
(Name of Attorney or Agent)
& ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025
and direct telephone calls to Robert g. Winkle, Intel, (503)264-8080.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Qing Ma

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Second/Joint Inventor Jin Lee

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Third/Joint Inventor Harry Fujimoto

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Fourth/Joint Inventor Changhong Dai

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Fifth/Joint Inventor Shiuh-Wuu Lee

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Sixth/Joint Inventor Travis Eiles

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Seventh/Joint Inventor Krishna Seshan

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
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